## REMARKS

Claims 1-27 are pending in the application.

Claims 1-27 are rejected.

Claims 1, 8, 14, 20 and 26-27 are amended.

Reconsideration and allowance of claims 1-27 is respectfully requested in view of the following.

***Responses to Rejections to Claims – 35 U.S.C. §103***

Claims 1-7, 10-19 and 22-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Howard et al. (U.S. Patent No. 6,708,278) (Howard hereinafter) in view of Shishizuka et al. (U.S. Patent No. 6,347,202) (Shishizuka hereinafter). Claims 8-9 and 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Howard et al. (U.S. Patent No. 6,708,278) (Howard hereinafter) in view of Shishizuka et al. (U.S. Patent No. 6,347,202) (Shishizuka hereinafter), in further view of Applicant's Admitted Prior Art. This rejection is not applicable to the amended claims.

As the PTO recognizes in MPEP §2142:

> The Examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. If the Examiner does not produce a *prima facie* case, the applicant is under no obligation to submit evidence of nonobviousness.

The USPTO clearly cannot establish a *prima facie* case of obviousness in connection with the amended claims for the following reasons:

35 U.S.C. §103(a) provides that:

> [a] patent may not be obtained...if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.... (emphasis added)

Thus, when evaluating a claim for determining obviousness, all limitations of the claim must be evaluation. However, the references, alone, or in any combination, do not teach all limitations.

*Howard in view of Shishizuka*

Claims 1-7, 10-19 and 22-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Howard in view of Shishizuka. This rejection is not applicable to the claims.

Independent claim 1 includes, "coupling a bus mastering device to a bus mastering device controller via a bus; coupling the bus mastering device controller to an IHS; detecting an access request for the bus mastering device, wherein the detecting is performed by a processor of the IHS; and in response to failing to detect an access request for the bus mastering device within a predetermined period of time, suspending the bus mastering device controller associated with the bus mastering device, wherein the now suspended controller no longer prevents the processor from entering low power states." Howard does not teach coupling a bus mastering device to a bus mastering device controller via a bus, coupling the bus mastering device controller to an IHS, detecting an access request for the bus mastering device, wherein the detecting is performed by a processor of the IHS, and in response to failing to detect an access request for the bus mastering device within a predetermined period of time, suspending the bus mastering device controller associated with the bus mastering device, wherein the now suspended controller no longer prevents the processor from entering low power states.

According to the Office Action, Howard teaches "in response to detecting that a bus mastering device is not needed, suspending a bus mastering device controller [col. 3, lines 34-45], wherein the now suspended controller no longer prevents the processor from entering low power states [col. 6, lines 42-62]." page 2, lines 8-12. Howard teaches nothing about suspending a bus mastering device controller associated with a bus mastering device in response to failing to detect an access request for the bus mastering device within a predetermined period of time. Instead, Howard teaches awakening bus circuitry from an inactive state. According to Howard, "the invention relates to apparatus and techniques for awakening bus circuitry from an inactive state as needed." col. 4, lines 63-64. Additionally, Howard does not teach that the detecting is performed by a processor of the IHS. As such, Howard teaches nothing about suspending a bus mastering device controller associated with a bus mastering device in response to failing to detect an access request for the bus mastering device within a predetermined period of time.

Additionally, Howard teaches nothing about the now suspended controller no longer preventing the processor from entering low power states. More specifically, Howard does not teach a controller preventing a processor from entering low power states. Instead, Howard teaches a system that can place various components in a shutdown state. According to

Howard, "the operating system or the power manager 210, can place various components in a shutdown state (or sleep mode) so as to conserve power." col. 6, lines 46-49. As such, Howard does not teach a bus mastering device controller that prevents a processor from entering a lower power state.

As discussed above, Howard fails to teach key limitations of claim 1. Shishizuka does not make up for those deficiencies. Shishizuka does not teach detecting an access request for a bus mastering device, wherein the detecting is performed by a processor of the IHS, and wherein a bus mastering device controller is suspended. At best, Shishizuka teaches detecting a request for a bus agent, wherein the detecting is performed by the bus agent, and wherein the bus agent is suspended. According to Shishizuka, "the bus agent detects an activity of a bus" and "has three states of sleep, wakeup and wait" and that "when a request is issued, the bus agent returns to the wakeup state" and when there is "no request, the bus agent shifts to the sleep state." Fig. 88. As such, Shishizuka does not teach a processor of the IHS detecting an access request for a bus mastering device, wherein the detecting is performed by a processor of the IHS, and wherein a bus mastering device controller is suspended as is currently claimed.

Additionally, Shishizuka teaches nothing about suspending a bus mastering device controller associated with a bus mastering device in response to failing to detect an access request for a bus mastering device within a predetermined period of time. In fact, Shishizuka does not even teach a bus mastering device controller associated with a bus mastering device. Instead, Shishizuka teaches a bus agent, as illustrated in Fig. 88.

Furthermore, Shishizuka does not teach coupling a bus mastering device to a bus mastering device controller via a bus, and the Office Action has made no argument to the contrary. Shishizuka at Figure 88 shows a bus agent, and does not show a bus mastering device coupled to a bus mastering device controller via a bus.

For at least these reasons, the USPTO's burden of factually supporting a prima facie case of obviousness clearly cannot be met with respect to claim 1. Independent claims 14, 26 and 27 are allowable at least for similar reasons as described for representative claim 1.

*Howard in view of Shishizuka and in view of Applicant's Admitted Prior Art*

Claims 8-9 and 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Howard in view of Shishizuka, in further view of Applicant's Admitted Prior Art. This rejection is not applicable to the claims.

As discussed above, Howard and Shishizuka fail to teach key limitations of claim 1. Applicant's Admitted Prior Art does not appear to make up for those deficiencies, and the Office

Action has made no argument to the contrary. For at least this reason, the USPTO's burden of factually supporting a prima facie case of obviousness clearly cannot be met with respect to claim 1. Independent claims 14, 26 and 27 are allowable at least for similar reasons as described for representative claim 1.

Therefore, it is impossible to render the subject matter of the claims as a whole obvious based on a single reference or any combination of the references, and the above explicit terms of the statute cannot be met. As a result, the USPTO's burden of factually supporting a *prima facie* case of obviousness clearly cannot be met with respect to the claims, and a rejection under 35 U.S.C. §103(a) is not applicable.

There is still another compelling, and mutually exclusive, reason why the references cannot be combined and applied to reject the claims under 35 U.S.C. §103(a).

The PTO also provides in MPEP §2142:

> [T]he Examiner must step backward in time and into the shoes worn by the hypothetical "person of ordinary skill in the art" when the invention was unknown and just before it was made. In view of all factual information, the Examiner must then make a determination whether the claimed invention "as a whole" would have been obvious at that time to that person. ...[I]mpermissible hindsight must be avoided and the legal conclusion must be reached on the basis of the facts gleaned from the prior art.

Recently, the Supreme Court ruled that the "teaching, suggestion, or motivation (TSM) test" for determining obviousness still applies, but should be used in a more "expansive and flexible" manner. *KSR Int'l. Co. v. Teleflex Inc.*, 550 U.S. __, 11 (2007). The Court stated that "a patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art. Although common sense directs one to look with care at a patent application that claims as innovation the combination of two known devices according to their established functions, it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does. This is so because inventions in most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known." Id. at 14-15, emphasis added.

In the present case, the Examiner has not expressed a reason why a person of ordinary skill in the art would combine Howard, Shishizuka and Applicant's Admitted Prior Art as required by independent claim 1. Howard does not disclose in response to failing to detect an access

request for a bus mastering device within a predetermined period of time, suspending a bus mastering device controller associated with the bus mastering device, wherein the now suspended controller no longer prevents the processor from entering low power states. Shishizuka does not disclose in response to failing to detect an access request for a bus mastering device within a predetermined period of time, suspending a bus mastering device controller associated with the bus mastering device, wherein the now suspended controller no longer prevents the processor from entering low power states. Applicant's Admitted Prior Art does not disclose in response to failing to detect an access request for a bus mastering device within a predetermined period of time, suspending a bus mastering device controller associated with the bus mastering device, wherein the now suspended controller no longer prevents the processor from entering low power states. If Howard, Shishizuka, and Applicant's Admitted Prior art are combined as suggested by the Office Action, the result would not be as is required by the claims. The claims require in response to failing to detect an access request for a bus mastering device within a predetermined period of time, suspending a bus mastering device controller associated with the bus mastering device, wherein the now suspended controller no longer prevents the processor from entering low power states.

Therefore, independent claims 1, 14, 26 and 27, and their respective dependent claims are submitted to be allowable.

The amended claims are supported by the specification.

In view of all of the above, the allowance of claims 1-27 is respectfully requested.

The Examiner is invited to call the undersigned at the below-listed telephone number if a telephone conference would expedite or aid the prosecution and examination of this application.

Respectfully submitted,

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Dated: 7-20-07

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